Claims

1. An apparatus for receiving data of a source synchronous signal and a source synchronous clock signal in a source synchronous point-to-point communication system, said apparatus comprising:

a receiver circuit for receiving said data of said source synchronous signal; and

a feedback circuit for providing said receiver circuit with a plurality of feedback signals based on an output of said receiver circuit to synchronize receipt of said data of said source synchronous signal by said receiver circuit.

2. The apparatus of claim 1, wherein said receiver circuit comprises,

a first integrating detector circuit to integrate said data over a period of time relative to a first feedback signal of said plurality of feedback signals to produce a first output signal;

a second integrating detector circuit to integrate said data over a period of time relative to a second feedback signal of said plurality of feedback signals to produce a second output signal;

a third integrating detector circuit to integrate said data over a period of time relative to a third feedback signal of said plurality of feedback signals to produce a third output signal; and

a differentiating circuit coupled to said first integrating detector circuit and said second integrating detector circuit to determine a difference between said first output signal and said second output signal.

3. The apparatus of claim 1, wherein said feedback circuit comprises,

a filter to remove a voltage component of one of said receiver output signals to assert a filtered signal;

a voltage controlled oscillator for generating a plurality time varying signals; and

a phase interpolator to select one or more of a said plurality of time varying signals from said voltage controlled oscillator based on said filtered signal to provide said receiver with said plurality of feedback signals.

4. The apparatus of claim 2, wherein said first integrating detector circuit and said second integrating detector circuit and said third integrating detector circuit each comprise,

an integrating amplifier to integrate said data of said source synchronous signal relative to one of said plurality of feedback signals to determine a value for said data.

5. The apparatus of claim 2, wherein said first feedback signal of said plurality of feedback signals allows said first integrating detector circuit to determine if said data of said source synchronous signal is advanced in phase relative to said source synchronous clock signal of said source synchronous point-to-point communication system.

6. The apparatus of claim 2, wherein said second feedback signal of said plurality of feedback signals allows said second integrating detector circuit to determine if said data of said source synchronous signal is delayed in phase relative to said source synchronous clock signal of said source synchronous point-to-point communication system.

7. The apparatus of claim 2, wherein said third feedback signal of said plurality of feedback signals allows said third integrating detector circuit to integrate said data of said source synchronous signal relative to an in phase version of said source synchronous clock signal relative to said data.

8. The apparatus of claim 1, wherein said source synchronous signal comprises a multi-level source synchronous signal.

9. The apparatus of claim 3, wherein said voltage component is an alternating current voltage.

10. The apparatus of claim 1, wherein said source synchronous signal is a differential signal.

11. The apparatus of claim 8, wherein said multi-level source synchronous signal comprises one of a two-level pulse amplitude modulation signal and a four-level pulse amplitude modulation signal.

12. A method for continuously synchronizing a source synchronous clock signal on a clock line with a data signal on a data line at a receiver of said source synchronous clock signal and said data line, said method comprising the steps of:

determining at said receiver a phase relationship between said source synchronous clock signal and said data signal each time said receiver receives said source synchronous clock signal and said data signal, and

synchronizing said source synchronous clock signal and said data signal to be in phase at said receiver each time said receiver receives said data signal and said source synchronous clock signal, wherein said synchronization is based on said determined phase relationship between said source synchronous clock signal and said data signal to continuously synchronize said source synchronous clock signal and said data signal to allow said receiver to integrate said data signal over an entire period of said clock signal.

13. The method of claim 12, wherein said phase relationship between said source synchronous clock signal and said data signal is determined by the steps of:

shifting said source synchronous clock signal in a first direction relative to said source synchronous clock signal as received by said receiver and integrating said source synchronous clock signal shifted in said first direction together with said data signal to produce a first output signal;

shifting said source synchronous clock signal in a second direction relative to said source synchronous clock signal as received by said receiver and integrating said source synchronous clock signal shifted in said second direction together with said data signal to produce a second output signal; and

determining a magnitude difference between said first output signal and said second output signal to determine said phase relationship between said source synchronous clock signal and said data signal.

14. The method of claim 13, further comprising the steps of,

shifting said source synchronous clock signal in a desired direction based on said magnitude difference between said first output signal and said second output signal to synchronize an edge of said data signal with an edge of said source synchronous clock signal; and

integrating said source synchronous clock signal synchronized to said data signal over an entire period of said source synchronous clock signal to determine a value for said data signal.

15. The method of claim 13, wherein a phase interpolator circuit based on said magnitude difference between said first output signal and said second output signal selects from a voltage controlled oscillator a first course clock signal and a second course clock signal to generate said source synchronous clock signal shifted in said first direction and said source synchronous clock signal shifted in said second direction.

16. The method of claim 15, wherein said phase interpolator circuit further generates said source synchronous clock signal synchronized to said data signal based on said magnitude difference between said first output signal and said second output signal.

17. The method of claim 13, wherein a differential amplifier determines said magnitude difference between said first output signal and said second output signal.

18. The method of claim 13, further comprising the step of filtering said determined magnitude difference between said first output signal and said second output signal to remove a particular voltage component of said determined magnitude difference.

19. The method of claim 15, wherein said source synchronous clock signal drives said voltage controlled oscillator to provide said phase interpolator circuit with said first course clock signal and said second course clock signal to allow said phase interpolator circuit to generate said source synchronous clock signal shifted in said first direction,

said source synchronous clock signal shifted in said second direction, and said source synchronous clock signal synchronized to said data signal.

20. The method of claim 15, wherein said source synchronous clock signal drives a phase lock loop circuit to provide said phase interpolator circuit with a plurality of signals to allow said phase interpolator circuit to generate said source synchronous clock signal shifted in said first direction, said source synchronous clock signal shifted in said second direction, and said source synchronous clock signal synchronized to said data signal.

21. The method of claim 12, wherein said data signal is a differential signal.

22. The method of claim 12, wherein said source clock signal is a differential clock signal.

23. The method of claim 12, wherein said data signal comprises a multi-level source synchronous signal.

24. The method of claim 23, wherein said multi-level source synchronous signal comprises one of a two-level pulse amplitude modulation signal and a four-level pulse amplitude modulation signal.